

In the claims:

Please amend the claims as follows:

Claims 1-3 (cancelled).

Claim 4 (previously amended): The display of claim 17, wherein in order to install said control circuit in a control circuit accommodation portion of said TFT substrate, said control circuit accommodation portion is made thinner than other portions of said TFT substrate.

Claim 5 (cancelled).

Claim 6 (previously amended): The display of claim 17, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

Claims 7-12 (cancelled).

Claim 13 (previously amended): The method of claim 24, further comprising the step of thinning a portion of said counter substrate which is located opposite to a control circuit for controlling said driver circuit made up of said driver TFTs, to install said control circuit.

Claim 14 (previously amended): The method of claim 24, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

Claims 15-16 (cancelled).

Claim 17 (currently amended): An active matrix liquid crystal display comprising:  
a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;  
a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing over said liquid crystal material and provided between said first substrate and said counter substrate; and

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate.

Claims 18-20 (cancelled).

Claim 21 (currently amended): An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing over said liquid crystal material and provided between said first substrate and said counter substrate; and

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate.

Claim 22 (currently amended): An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing over said liquid crystal material and provided between said first substrate and said counter substrate, said sealing material being provided outside at least said pixel TFTs; and

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate.

Claim 23 (currently amended): An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing over said liquid crystal material and provided between said first substrate and said counter substrate, said sealing material being provided outside at least said pixel TFTs; and

a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate.

Claim 24 (currently amended): A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing over said liquid crystal material and provided between said first substrate and said counter substrate and outside at least said pixel TFTs; and  
a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate,  
said method comprising:  
cutting said first substrate and said counter substrate outside said sealing material having said control circuit under and in contact with said sealing material.

Claim 25 (currently amended): A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;  
a bus line provided over said first substrate and connected with at least one of said pixel TFTs;  
a counter substrate located opposite to said first substrate;  
a layer of a liquid crystal material provided between said first substrate and said counter substrate;  
a sealing material sealing over said liquid crystal material and provided between said first substrate and said counter substrate; and  
a control circuit comprising a control circuit chip provided under and in contact with said sealing material, said control circuit provided over said first substrate,  
said method comprising:  
cutting said first substrate and said counter substrate outside said sealing material having said control circuit under and in contact with said sealing material.

Claims 26-29 (cancelled).

Claim 30 (previously added): The display of claim 21, wherein in order to install said control circuit in a control circuit accommodation portion of said TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

Claim 31 (previously amended): The display of claim 21, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

Claims 32-34 (cancelled).

Claim 35 (previously added): The display of claim 22, wherein in order to install said control circuit in a control circuit accommodation portion of said TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

Claim 36 (previously amended): The display of claim 22, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

Claims 37-39 (cancelled).

Claim 40 (previously added): The display of claim 23, wherein in order to install said control circuit in a control circuit accommodation portion of said TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

Claim 41 (previously amended): The display of claim 23, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

Claim 42 (previously added): The method of claim 25, wherein said cutting step is carried out in such a way that said cut side edges to which said nonconductive or weakly conductive material is applied or adhesively bonded are parallel or vertical to a direction of array of said pixel TFTs.

Claim 43 (cancelled).

Claim 44 (previously added): The method of claim 25, further comprising the step of thinning a portion of said counter substrate which is located opposite to said control circuit, to install said control circuit.

Claims 45-60 (cancelled).

Claim 61 (previously amended): A semiconductor device comprising:  
a pixel TFT provided over a first substrate comprising a glass;  
a channel formation region provided in a semiconductor film provided over said first substrate;  
a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;  
a counter substrate located opposite to said first substrate;  
a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;  
a sealing material provided between said first substrate and said counter substrate;  
and  
a nonconductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,  
wherein said nonconductive material is provided on an outer side of said sealing material, and  
wherein said gate insulating film has a thickness of 500 to 2000 Å.

Claim 62 (previously amended): A semiconductor device comprising:  
a pixel TFT provided over a first substrate comprising a glass;  
a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate;

and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

Claim 63 (previously amended): A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said first substrate;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate;

and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

Claim 64 (previously amended): A semiconductor device comprising:  
a pixel TFT provided over a first substrate comprising a glass;  
a channel formation region provided in a semiconductor film provided over said first substrate;  
a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;  
a driver TFT provided over said first substrate;  
a counter substrate located opposite to said first substrate;  
a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;  
a sealing material provided between said first substrate and said counter substrate;  
and  
a weakly conductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,  
wherein said weakly conductive material is provided on an outer side of said sealing material, and  
wherein said gate insulating film has a thickness of 500 to 2000 Å.

Claims 65-68 (cancelled).

Claim 69 (previously amended): The display of claim 61 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.



Claim 70 (previously amended): The display of claim 62 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

Claim 71 (previously amended): The display of claim 63 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

Claim 72 (previously amended): The display of claim 64 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.